REMARKS

Claims 21-24 and 26-43 have been examined, with all claims rejected.

Applicant thanks the Examiner for the indication of allowable subject matter in claims 24 and 29.

Independent claims 21 and 41-43 have been amended to specify that a control unit or control means is configured to apply the data signal to the gate terminal of the logic field effect transistor before the clock signal is switched to a level that activates the clock pulse field effect transistor. This amendment is supported, for example, by now cancelled claim 33 and page 15, lines 31-37, of the originally filed specification.

Claim 23 has been similarly amended.

Drawing Objection; and Claim Rejections under 35 U.S.C. § 112, First Paragraph

The drawings remain objected to because it is the Examiner's position that the claimed control unit/means recited in claims 21 and 41-43 is not shown in the drawings. Also, claims 21-24 and 26-43 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement, because it is the Examiner's position that the specification does not disclose the claimed control unit/means.

Figures 2, 4, and 5 are amended to show that the control unit/means recited in claims 21 and 41-43 is coupled to the clock signal.

Support for this amendment can be found in page 15, lines 31-37, of the originally filed specification, where it is mentioned that the control unit can be set up in such a manner that it applies the data signal to the gate terminal of the logic field effect before the clock signal is switched for changing the clock pulse field effect transistor from a state with electrically nonconducting channel region into a state with electrically conducting channel region.

Reconsideration and withdrawal of this objection and rejection are respectfully requested.

Claim Objections

Claims 34-40 have been objected to because of informalities.

The Examiner bases this objection on claim 34 being dependent form claim 30. Claim 34, however, was amended to be dependent from claim 21 in the previous Office Action. Applicant respectfully submits that claim 34 is of proper dependent form. Claims 35-40 which are dependent on amended claim 34 are also in proper dependent form.

Reconsideration and withdrawal of this objection are therefore respectfully requested.

Claim Rejections – 35 U.S.C. § 102

Claims 21-23, 26-28, and 30-43 remain rejected under 35 U.S.C. § 102(b) as being anticipated by Kim (U.S. Patent No. 6,486,719).

Kim does not disclose "...a control unit configured to apply the data signal to the gate terminal of the logic field effect transistor before the clock signal is switched to a level that activates the clock pulse field effect transistor such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated," as required by amended independent claim 21.

In Kim, a latch circuit 41a of Figure 6 has NMOS transistors NA and NB connected in series with each other and in parallel with NMOS pull-down transistor N1. Both the NMOS transistors NA and NB are turned on in combination with the NMOS pull-down transistor N1. See Kim, column 5, lines 51-60.

A latch circuit 41d shown in Figure 9 is a modification of the latch circuit 41a of Figure 6. The latch circuit 41d of Figure 9 has NMOS transistors NA and NB connected in series with each other and in parallel with NMOS pull-down transistor N0. NMOS pull-down transistor N1 is connected in series with the parallel circuit of the serially connected NMOS transistors NA and NB and the NMOS pull-down transistor N0.

Since the latch circuit 41d of Figure 9 is a modification of the latch circuit 41a of Figure 6, the operation of the latch circuit 41d of Figure 9 is similar to the operation of the latch circuit 41a of Figure 6. Therefore, the latch circuit 41d of Figure 9 turns on both the NMOS transistors NA and NB in combination with the NMOS pull-down transistor N0.

Assuming that the NMOS transistor NA corresponds to the clock pulse field effect transistor, the NMOS transistor NB corresponds to the logic field effect transistor, and the NMOS pull-down transistor N1 corresponds to the feedback field effect transistor, Kim does not disclose that the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated.

Independent claim 21 and dependent claims 22-24 and 26-40 are therefore novel over Kim.

Since independent claims 41-43 include limitations similar to the limitations discussed above with respect to independent claim 21, they are patentable over Kim for at least the same reasons.

Reconsideration and withdrawal of the prior art rejection are respectfully requested.

In view of the above, Applicant believes the pending application is in condition for allowance.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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